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Fabrication and AC Performance of Flexible Indium-Gallium-Zinc-Oxide Thin-Film Transistors

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The internet of things or foldable phones call for a variety of flexible sensor conditioning and transceiver circuits. However, the realization of high-performance, large-area, and deformable analog circuits is limited by the materials and the processes compatible with mechanically flexible substrates. Among the different semiconductors, InGaZnO is one of the most promising materials to realize high-frequency flexible thin-film transistors (TFTs) and circuits. In this work, the effect of different geometries, including self-aligned, vertical, and double-gate structures on the AC behaviour of flexible IGZO TFTs is presented. All TFTs are based on Al₂O₃ insulating layers, InGaZnO semiconductor, and polyimide substrates. The presented TFTs exhibit state-of-the-art performance including a field-effect mobility up to 15 cm²/Vs and a mechanical bendability down to radii of 3.5 mm. Due to different trade-offs required in the fabrication, flexible IGZO TFTs with the shortest channel length of 160 nm do not exhibit the highest measured frequency, whereas exceptional maximum oscillation and transit frequencies of 304 MHz and 135 MHz are demonstrated for 500 nm long self-aligned TFTs. Such optimized transistors can be used to realize entirely flexible analog circuits leading towards imperceptible electronic systems.

Introduction

Flexible and conformable devices operated in contact with the human body, or fabricated using cost-effective roll-to-roll techniques are one of the next major steps in the development of consumer electronics (1). Specifically, flexible transistors promise to enable new applications, including rollable display backplanes and active RFID tags. Additionally, analog circuits such as amplifiers, buffers, or transceivers made from flexible transistors can be used to realize front-end conditioning and sensor readout circuits for unobtrusive, wearable devices (2). In this context, it is important to develop bendable thin-film transistors (TFTs) suitable for operation at frequencies ≥ 10 MHz. At this aim, several groups have reported flexible transistors based on high-performance materials such as black phosphorus (3), molybdenum disulphide (MoS₂) (4), graphene (5), or silicon nano-membranes (6), demonstrating impressive transit frequencies close to 100 GHz. However, these materials and the associated deposition techniques exhibit only limited scalability. TFTs based on amorphous semiconductors, especially Indium-Gallium-Zinc-Oxide (IGZO) (7), are particularly suitable to realize electronics on large-area polymer substrates.

IGZO outperforms other scalable semiconductors like amorphous silicon and organic materials when bendability and electrical performance are required simultaneously (2). However, the AC performance of flexible IGZO TFTs is limited by parasitic resistances and capacitances, as well as by the lateral TFT dimensions and the difficulty to reliably fabricate features smaller than $\approx 1\ \mu\text{m}$ on polymer substrates. Here, multiple approaches to improve the AC performance of flexible IGZO TFTs, including bottom-gate, vertical and double-gate transistor geometries in combination with self-alignment, focused ion beam (FIB), and direct laser writing (DLW) fabrication techniques, are presented and discussed.

Flexible IGZO TFT technology

All transistors were fabricated on free standing $50\ \mu\text{m}$ thick polyimide substrates with a surface area of $7.5\ \text{cm} \times 7.5\ \text{cm}$. Prior to the fabrication, the substrates were cleaned with acetone and IPA and pre-baked in a vacuum oven for 24 h to evaporate absorbed solvents and water. Additionally, both sides of the substrates were coated with $50\ \text{nm}$ SiN to improve the adhesion and to prevent outgassing of the polyimide, using plasma enhanced chemical vapour deposition. Metallic contacts and interconnection lines were deposited by e-beam evaporation: Source and drain contacts were made from Au plus Ti or Cr adhesion layers, whereas gate contacts were made from either Cr, Ti or Cu. Transparent contacts were made from ITO, sputtered using an RF source and Ar gas. The employed semiconductor was amorphous Indium-Gallium-Zinc-Oxide (IGZO), which was RF sputtered using a ceramic target with a stoichiometric composition of In:Ga:Zn:O = 1:1:1:4, and a pure Ar atmosphere. Insulating layers acting as gate oxide and device passivation were deposited in an atomic layer deposition chamber using trimethylaluminium and water as Aluminium and Oxygen precursors, respectively. The resulting Al_2O_3 had a dielectric constant of 9.5 and formed a high-quality interface with IGZO. The highest temperature involved in this fabrication process was 150°C , which was required for the ALD deposition of Al_2O_3 . To ensure compatibility of the manufacturing process with a wide range of polymer substrates, no additional annealing steps were performed. A fully processed substrate is shown in Fig. 1a.

The layout of the TFTs was optimized to ensure a reliable AC and DC characterisation. Therefore, the ground-signal-ground (GSG) contact pad layout shown in Fig. 1b and Fig. 1c employing $100\ \mu\text{m}$ pads with a $150\ \mu\text{m}$ spacing was used.

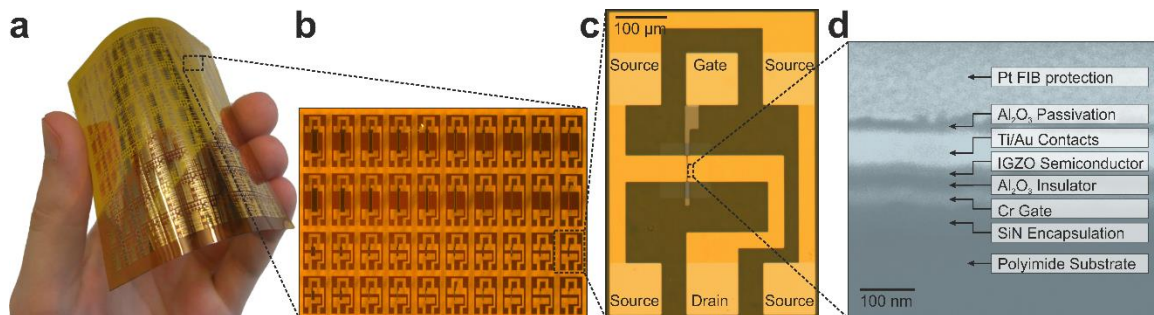


Figure 1. Conventional bottom-gate IGZO TFTs on a polyimide foil: a) Picture of a fully processed substrate. b) Micrograph of a unit cell containing 40 TFTs. c) Micrograph of a single transistor with ground-signal-ground contacts. d) Cross-sectional SEM image of a TFT cut by a focused ion beam showing all device layers.

TFT channel geometries

To realize flexible TFTs for analog high-speed applications, multiple factors need to be considered. Here, the transit frequency f_T is used as a figure of merit to judge the frequency performance of a field-effect transistor:

$$f_T = \frac{g_m}{2\pi \cdot C_G} \propto \frac{\mu_{eff}}{L \cdot (L + 2 \cdot L_{OV})} \quad [1]$$

It is defined as the frequency at which the magnitude of the small-signal current gain equals unity. In particular, g_m is the transconductance of the TFT (which takes also the contact resistance into account), C_G the gate capacitance, μ_{eff} the effective field effect mobility, L the channel length, and L_{OV} the gate to source or drain overlap length.

All lateral geometrical feature sizes are limited by the deformation of the flexible plastic substrate during the fabrication process. Such deformation is generally caused by thermal expansion and stress induced by the deposition of different material layers, as well as absorption of various liquids during the fabrication process. For example, the used polyimide has a coefficient of thermal expansion of $12 \times 10^{-6} /K$ and a humidity expansion coefficient of $9 \times 10^{-6} /\%RH$ (8). The resulting variation of the substrate size during the fabrication process calls for tolerances to ensure a successful alignment of the different device layers. Furthermore, these mechanical instabilities also complicate the large-area fabrication of lateral features with sizes below $\approx 1 \mu m$. Since the alignment of the source and drain contacts relative to the gate contact is the most critical alignment step for most TFTs, corresponding gate to source/drain overlaps are required. In the electrical domain, gate to source/drain overlaps have two competing effects. First, as indicated in Equation 1, these overlaps cause parasitic overlap capacities and hence reduce the frequency performance. Secondly, gate to source/drain overlaps also affect the contact resistance, which in turn influences the effective field effect mobility and thus the transconductance. With respect to the contact resistance, large overlaps are required to reduce the contact resistance and thereby maximize the effective mobility. Therefore, while shorter channels are always beneficial for high speed TFTs, it is not always obvious what the optimal overlaps to maximize the transit frequency are (9).

Since the minimum feature size as well as the quality of contacts, and hence the contact resistance, is significantly influenced by the device structure and fabrication technique, different approaches to realize flexible high-speed IGZO TFTs have been evaluated. As shown in Fig. 2, these include various planar TFTs manufactured by UV lithography, vertical geometries, and transistors fabricated using sequential structuring.

Conventional bottom gate inverted staggered TFTs. These devices are fabricated using standard photolithography. A cross-sectional SEM image is provided in Fig. 1d, and their device structure is shown in Fig 2a. If fabricated on free-standing large area substrates ($\geq 10 \text{ cm}^2$) the lateral dimensions are typically limited to $\approx 5 \mu m$. Nevertheless, optimized devices with feature sizes down to $1 \mu m$ can be realized by attaching the substrates to a rigid glass carrier support during the mask alignment steps (10).

Vertical TFTs. Here, the source and drain contacts are fabricated on top of each other and separated by a SiN spacing layer (Fig 2b). The resulting channel length is either vertical (11), or quasi vertical (12) and can be as short as 300 nm.

Self-aligned TFTs. Fig. 2c shows the layer structure of a TFT with self-aligned source and drain contacts. This is achieved by resist exposure through the semi-transparent polyimide substrate using the opaque bottom gate contact as a mask. The resulting devices

can exhibit channel length down to 500 nm and gate overlaps of 1.5 μm without any misalignment (13).

Self-aligned double gate. By replacing the opaque Au source/drain contacts of self-aligned TFTs with transparent ITO, a second self-aligned top-gate can be deposited (14). The resulting double-gate TFTs shown in Fig. 2d have a limited channel length of $\approx 4 \mu\text{m}$. Here the top and bottom gate are electrically connected to increase the channel capacitance and hence g_m . The two gates are not controlled independently.

Sequential structuring TFTs. Sequential structuring has only limited use for large area fabrication but enables the utilisation of alternative nano-fabrication techniques. TFTs with dimensions down to 160 nm were fabricated by ion beam milling (FIB) of the channel. As shown in Fig. 2e, these TFTs are not passivated and contain overlaps of $\approx 2 \mu\text{m}$. Alternatively, direct laser writing (DWL) can be used to define the channel dimensions of top gate TFTs (15). Such TFTs exhibit channel length down to 280 nm and gate overlaps down to 2.6 μm .

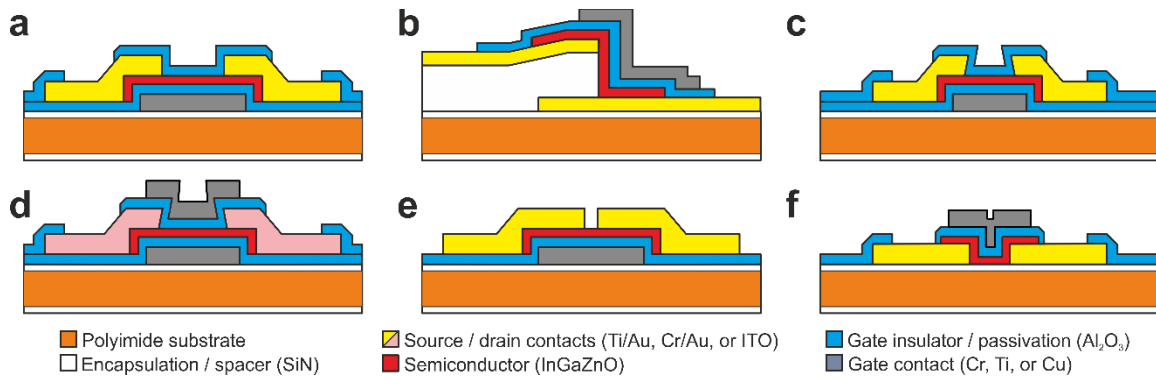


Figure 2. Schematic structure of the fabricated flexible IGZO TFTs: a) Conventional bottom-gate (10), b) vertical (12), c), self-aligned (13), d) double-gate self-aligned (14), e) focused ion beam structured, f) direct laser written (15).

Transistor performance

TFTs were characterized under ambient conditions using an Agilent technologies B1500A parameter analyser. Performance parameters were extracted from the measurements in the saturation regime using standard Shichman-Hodges MOSFET model (16).

Electrical performance

Representative DC characteristics of a conventional bottom-gate TFT are shown in Fig. 3. The transfer characteristics shown in Fig. 3a displays the TFT performance in the linear ($V_{DS} = 0.1 \text{ V}$) and in the saturation ($V_{DS} = 5 \text{ V}$) regime. The device exhibits state of the art performance including a typical field effect mobility of $\approx 15 \text{ cm}^2/\text{Vs}$, a threshold voltage of $\approx 1.2 \text{ V}$, an on-off current ratio $> 10^8$, and a subthreshold swing of $\approx 125 \text{ mV/dec}$. The output characteristic (Fig. 3b) confirms that the drain current saturates with a width normalized drain conductance $< 28 \text{ nS}/\mu\text{m}$. This leads to an internal transistor gain of 275 at $V_{GS} = 3 \text{ V}$. All the TFT values correspond well with the TFT dimensions, and the specific capacitance of the 25 nm thick Al_2O_3 gate insulator. The measured gate capacitance is shown in Fig. 3c. It is important to notice that the measured gate capacitance is smaller for

higher measurement frequencies. This is because present trap states cannot be occupied and de-occupied fast enough at high measurement frequencies.

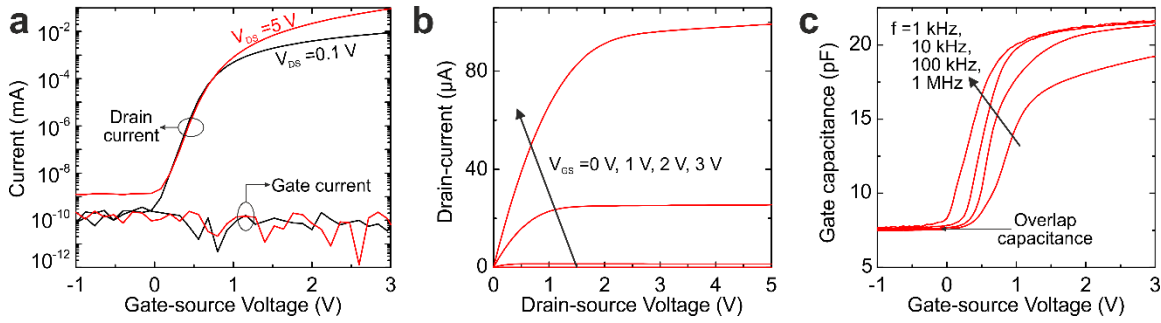


Figure 3. DC performance of a flexible IGZO TFT with a channel width of 50 μm and a channel length of 4 μm . a) Transfer characteristic, b) Output characteristic, and c) Gate capacitance measured at different frequencies.

Mechanical performance

To assess the mechanical properties of the fabricated flexible IGZO TFTs, the devices were characterized under strain. Tensile and compressive strain was induced by bending the devices parallel to the TFT channels (Fig. 4a). Bending down to radii of 0.7 mm was done by wrapping the TFTs around rods of different diameter or by a custom-build automated bending machine. Strain values were calculated considering the bending radius as well as the thickness and Young's moduli of the device layers (17).

Fig. 4b shows the normalized mobility of bottom-gate TFTs under mechanical strain. The measurement shows that the device mobility increases under tensile strain and decreases under compressive strain. Additionally, the threshold voltage decreases for tensile and increased for compressive strain. These effects are known and reflect the modification of the IGZO band structure caused by stretching or compressing covalent bonds (18). Fig. 4b also shows that the mobility drastically drops if the strain surpasses a critical point. The minimum bending radius for the presented TFTs is 3.5 mm (tensile) and 1.1 mm (compressive). While the described performance parameter shifts for low strain fully recover within ≈ 5 h, bending beyond the critical radius creates cracks and permanently damages the TFTs.

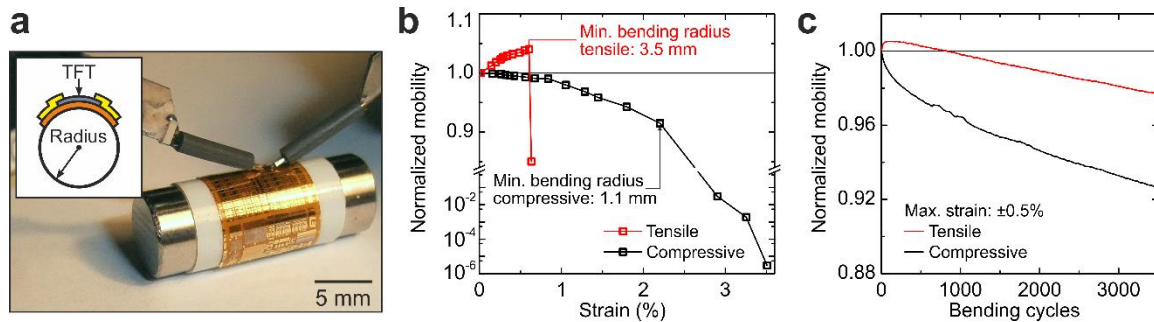


Figure 4. Mechanical performance of flexible IGZO TFTs: a) Photograph of a TFT characterized while bend parallel to the TFT channel. b) Influence of tensile and compressive strain on the TFT mobility. c) Influence of repeated tensile and compressive bending.

To evaluate the influence of repeated bending, the TFTs were bend and re-flattened up to 3500 times. Here, the maximum strain was 0.5%, corresponding to a radius of ≈ 4.5 mm, and the TFTs were measured while flat. Fig. 4c shows that the initial performance parameter shift is determined by the bending direction. Conversely, on the long term (>150 bending cycles), the effective mobility always decreases. This is a combination of electrical stress induced by the repeated measurement, and the formation of micro-cracks. Nevertheless, the observed shifts reach only 8%, and the TFTs stay fully functional.

Scaling and AC behaviour

The AC performances of all presented TFTs were evaluated by S-parameter measurements done by a HP 8753E network analyser.

Planar UV lithography TFTs

Planar TFTs manufactured using conventional UV lithography are the most common fabricated devices. These TFTs exhibit optimized interfaces which lead to comparably small contact resistances R_C between $5.6 \Omega\text{cm}$ (conventional TFTs with $15 \mu\text{m}$ overlap) to $12.4 \Omega\text{cm}$ (self-aligned TFTs with $1.5 \mu\text{m}$ overlap). Consequently, the dominant factor in Equation 1 is the gate capacitance, where a reduction of the lateral device dimensions is essential to enhance the frequency.

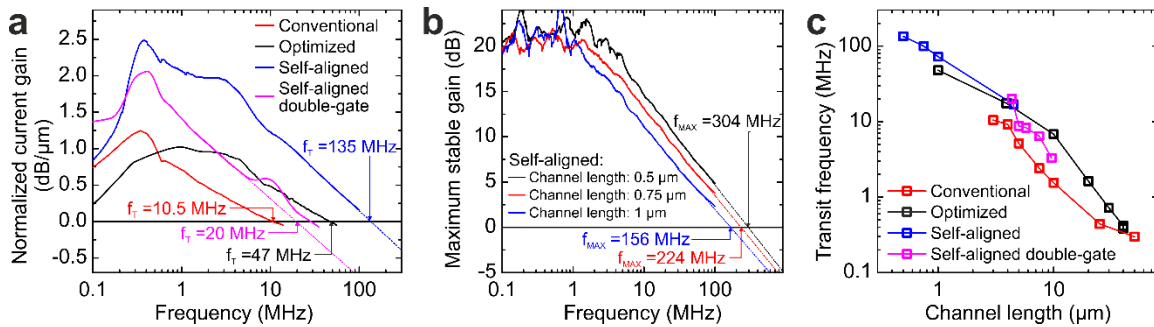


Figure 5. AC performance of planar TFTs fabricated using UV lithography. a) Measured current gain and resulting transit frequency for different TFT geometries, b) Maximum stable gain extracted from S-parameter measurements and resulting maximum oscillation frequency for self-aligned TFTs with varying channel length. c) Scaling behaviour of f_T versus channel length of different TFT geometries.

The performance of the different planar TFT geometries described above (conventional, optimized, self-aligned and self-aligned double-gate) is shown in Fig. 5a. All values are in line with the corresponding transconductance and gate capacitance measurements and do not significantly change under bending. Self-aligned bottom gate TFTs reach the highest transit frequency of 135 MHz. Here, the current gain (extracted from S-parameters of the respectively shortest TFT) was normalized for the channel width. The individual bias points were optimized to maximize the transit frequency (V_{DS} and V_{GS} varied between 2 V and 5 V). Nevertheless, the measurement also indicates the higher gain of self-aligned TFTs caused by the minimized channel length. Furthermore, also double gate TFTs exhibit a gain up to 2 dB/ μm which is caused by the increased gate capacitance improving the

transconductance. Fig. 5b shows that self-aligned bottom-gate TFTs also exhibit a high maximum oscillation frequency up to 304 MHz, and that this frequency scales with the channel length. In summary, Fig. 5c confirms that planar TFTs down to a channel length of 500 nm, always benefit from a reduction of the channel length. Furthermore, fabrication approaches resulting in smaller overlaps also improve the maximum frequency.

Vertical and sequential structuring TFTs.

Based on the results obtained from scaled conventional TFTs, alternative approaches to further reduce the transistor channel dimensions on flexible substrates were evaluated. Vertical TFTs appear to be an option since fully vertical TFTs with a channel length of 500 nm, and quasi vertical TFTs (Fig. 6a) with a channel length down to 300 nm could be successfully fabricated. The corresponding current gain measurement, plotted in Fig. 6b, demonstrates that f_T of vertical TFTs is limited to values of 80 kHz for vertical and 1.5 MHz for quasi vertical devices. Such small frequency values are mainly ascribed by the large overlaps of up to 17.8 μm which cause parasitic capacitances significantly larger than the channel capacitance. However, more importantly the increased contact resistances in the kilo-Ohm range result in an effective mobility of only 0.2 cm^2/Vs .

An alternative to realize short TFTs is the use of sequential writing techniques. First, flexible TFTs with a channel length down to 160 nm were fabricated using a FIB. In this case only the gap between the source and drain contacts was defined by a focused ion beam, whereas the overlap capacitance was not reduced. Furthermore, these TFTs suffer from serious short channel effects further limiting their f_T to a value of 5.8 MHz. Finally, direct laser writing partially combines the advantages of UV lithography and sequential writing techniques. Here a NanoScribe photonic professional two photon DWL system enables channel lengths down to 280 nm (Fig. 6c). However, the TFT fabrication process requires the fabrication of top-gate TFTs, which are typically known to exhibit a reduced effective mobility (19). While this approach results in acceptable contact resistances of 22 Ωcm , R_C is still higher than for all planar TFTs. This is reflected in Fig. 6d, where the measured current gain reveals a f_T of 80 MHz.

Here, it can be summarized that alternative device structures and fabrication techniques allow short channels down to 160 nm. Nonetheless, since the contact resistance becomes dominant for heavily scaled devices, further optimization is needed to take full advantage of the reduced device dimensions.

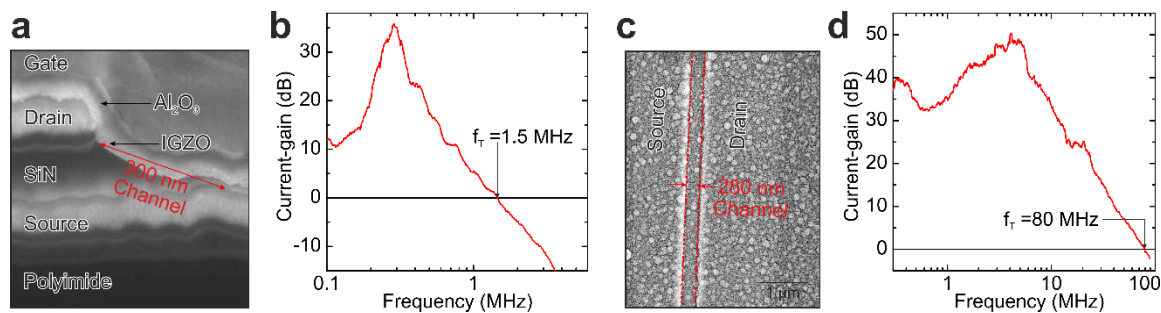


Figure 6. Alternative geometries and processes: a) FIB cross-sectional SEM micrograph, and b) current gain measurement of a quasi-vertical TFT. c) SEM micrograph, and d) current gain measurement of TFTs fabricated by direct laser writing.

Conclusion

Different methods to reduce the channel length and to improve the maximum operation frequency of flexible IGZO TFTs have been developed. As shown in Figure 7, these include TFTs defined by self-alignment, focused ion beam, and direct laser writing, as well as vertical and double-gate TFT structures. All devices are functional and exhibit channel length down to 160 nm.

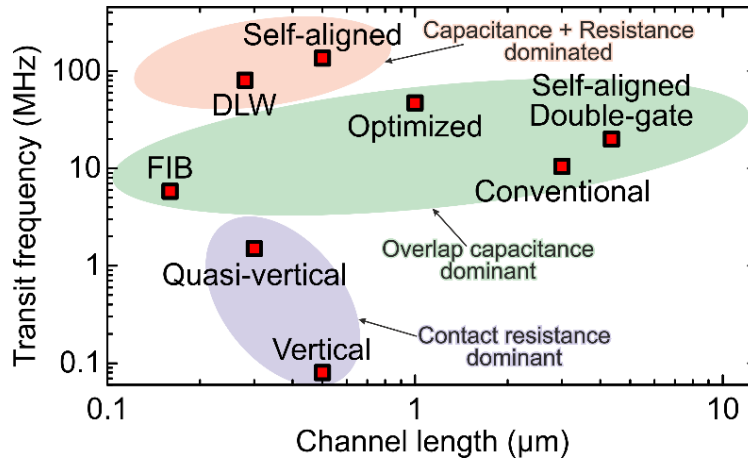


Figure 7. Impact of different fabrication approaches on the geometry and measured AC performance of flexible short channel IGZO TFTs.

It was found that although traditionally smaller feature structures are beneficial, a careful optimization of the gate capacitance, overlap capacitance, and contact resistance is required for high-frequency flexible IGZO TFTs. Consequently, the shortest transistors do not exhibit the highest transit frequency of 135 MHz, which is demonstrated for 500 nm long self-aligned flexible transistors. In this context, it has to be mentioned that in for 500 nm long self-aligned TFTs, the channel resistance R_{CH} is virtually identical to the contact resistance. This is because of the simultaneously short channels (reduces R_{CH}) and overlaps (increased R_C). This observation is in line with a mathematical model describing the transit frequency of heavily scaled IGZO TFTs (9). Since this model simultaneously considers parasitic capacitances and resistances it can be used to identify the dominant factor limiting f_T for different TFTs in Fig. 7. This shows that future improvements require the reduction of both, the contact resistances and the parasitic capacitances. Ultimately, flexible TFTs and circuits optimized to operate at frequencies significantly above 10 MHz, will open up the possibility to realize transceivers leading towards entirely flexible electronic systems (20, 21).

Acknowledgments

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